# 8041/8741
# UNIVERSAL PERIPHERAL INTERFACE
# 8-BIT MICROCOMPUTER

- **Fully Compatible with MCS-80™ and MCS-48™ Microprocessor Families**
- **Single Level Interrupt**
- **8-Bit CPU plus ROM, RAM, I/O, Timer and Clock in a Single Package**
- **Single 5V Supply**
- **Alternative to Custom LSI**
- **Pin Compatible ROM and EPROM Versions**
- **1K x 8 ROM/EPROM, 64 x 8 RAM, 18 Programmable I/O Pins**
- **Asynchronous Data Register for Interface to Master Processor**
- **Expandable I/O**

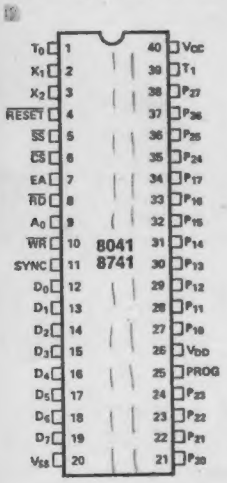
The Intel® 8041/8741 is a general purpose, programmable interface device designed for use with a variety of 8-bit microprocessor systems. It contains a low cost microcomputer with program memory, data memory, 8-bit CPU, I/O ports, timer/counter, and clock in a single 40-pin package. Interface registers are included to enable the UPI device to function as a peripheral controller in MCS-80™, MCS-85™, MCS-48™, and other 8-bit systems.

The UPI-41™ has 1K words of program memory and 64 words of data memory on-chip. To allow full user flexibility the program memory is available as ROM in the 8041 version or as UV-erasable EPROM in the 8741 version. The 8741 and the 8041 are fully pin compatible for easy transition from prototype to production level designs.

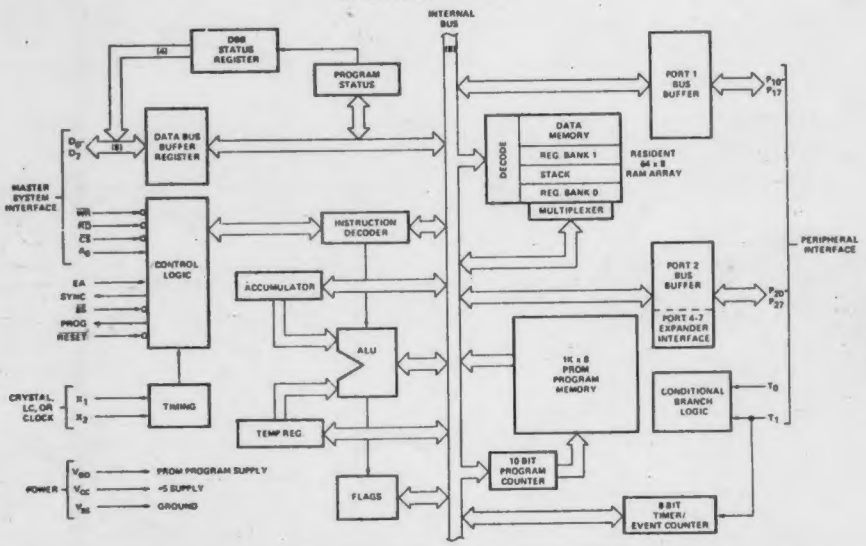
The device has two 8-bit, TTL compatible I/O ports and two test inputs. Individual port lines can function as either inputs or outputs under software control. I/O can be expanded with the 8243 device which is directly compatible and has 16 I/O lines. An 8-bit programmable timer/counter is included in the UPI device for generating timing sequences or counting external inputs. Additional UPI features include: single 5V supply, low power standby mode (in the 8041), single-step mode for debug (in the 8741), single level interrupt, and dual working register banks.

Because it's a complete microcomputer, the UPI provides more flexibility for the designer than conventional LSI interface devices. It is designed to be an efficient controller as well as an arithmetic processor. Applications include keyboard scanning, printer control, display multiplexing and similar functions which involve interfacing peripheral devices to microprocessor systems.

## PIN CONFIGURATION




## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin With
Respect to Ground ..... 0.5V to +7V
Power Dissipation ..... 1.5 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## D.C. AND OPERATING CHARACTERISTICS

$T_A$ = 0°C to 70°C, $V_{CC}$ = $V_{DD}$ = +5V ±5%, $V_{SS}$ = 0V

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{IL}$ | Input Low Voltage (All Except $X_1$, $X_2$) | -0.5 | | 0.8 | V | |
| $V_{IH}$ | Input High Voltage (All Except $X_1$, $X_2$ $\overline{RESET}$) | 2.0 | | $V_{CC}$ | V | |
| $V_{IH2}$ | Input High Voltage ($X_1$, $\overline{RESET}$) | 3.0 | | $V_{CC}$ | V | |
| $V_{OL}$ | Output Low Voltage ($D_0$-$D_7$, Sync) | | | 0.45 | V | $I_{OL}$ = 2.0 mA |
| $V_{OL2}$ | Output Low Voltage (All Other Outputs Except Prog) | | | 0.45 | V | $I_{OL}$ = 1.6 mA |
| $V_{OH}$ | Output High Voltage ($D_0$-$D_7$) | 2.4 | | | V | $I_{OH}$ = −400 μA |
| $V_{OH1}$ | Output High Voltage (All Other Outputs) | 2.4 | | | V | $I_{OH}$ = −50 μA |
| $I_{IL}$ | Input Leakage Current ($T_0$, $T_1$, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $A_0$, EA) | | | ±10 | μA | $V_{SS} \le V_{IN} \le V_{CC}$ |
| $I_{OL}$ | Output Leakage Current ($D_0$-$D_7$, High Z State) | | | ±10 | μA | $V_{SS} + 0.45 \le V_{IN} \le V_{CC}$ |
| $I_{DD}$ | $V_{DD}$ Supply Current | | 10 | 25 | mA | |
| $I_{CC} + I_{DD}$ | Total Supply Current | | 65 | 135 | mA | |
| $V_{OL3}$ | Output Low Voltage (Prog) | | | 0.45 | V | $I_{OL}$ = 1.0 mA |
| $I_{LI1}$ | Low Input Source Current $P_{10}$-$P_{17}$ $P_{20}$-$P_{27}$ | | | 0.4 | mA | $V_{IL}$ = 0.8V |
| $I_{LI2}$ | Low Input Source Current $\overline{RESET}$, SS | | | 0.2 | mA | $V_{IL}$ = 0.8V |

## A.C. CHARACTERISTICS

$T_A$ = 0°C to 70°C, $V_{CC}$ = $V_{DD}$ = +5V ±5%, $V_{SS}$ = 0V

**DBB Read:**

| Symbol | Parameter | 8741 | | 8041 | | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{AR}$ | $\overline{CS}$, $A_0$ Setup to $\overline{RD}$ ↓ | 60 | | 0 | | ns | |
| $t_{RA}$ | $\overline{CS}$, $A_0$ Hold After $\overline{RD}$ ↑ | 30 | | 0 | | ns | |
| $t_{RR}$ | $\overline{RD}$ Pulse Width | 300 | $2 \times t_{CY}$ | 250 | | ns | $t_{CY}$ = 2.5 μs |
| $t_{AD}$ | $\overline{CS}$, $A_0$ to Data Out Delay | | 370 | | 150 | ns | |
| $t_{RD}$ | $\overline{RD}$ ↓ to Data Out Delay | | 200 | | 150 | ns | |
| $t_{DF}$ | $\overline{RD}$ ↑ to Data Float Delay | 10 | | 10 | | ns | |
| | | | 140 | | 100 | ns | |
| $t_{RV}$ | Recovery Time Between Reads And/Or Write | 1 | | 1 | | μs | |
| $t_{CY}$ | Cycle Time | 2.5 | | 2.5 | | μs | 6 MHz Crystal |

MPU PERIPHERALS

**DBB Write:**

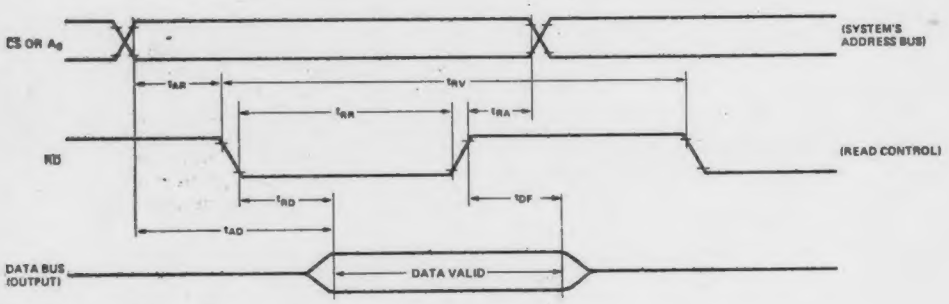
| Symbol | Parameter | 8741 | | 8041 | | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{AW}$ | $\overline{CS}$, $A_0$ Setup to $\overline{WR}$ ↓ | 60 | | 0 | | ns | |
| $t_{WA}$ | CS, $A_0$ Hold After WR ↑ | 30 | | 0 | | ns | |
| $t_{WW}$ | WR Pulse Width | 300 | $2 \times t_{CY}$ | 250 | | ns | $t_{CY} = 2.5\ \mu s$ |
| $t_{DW}$ | Data Setup to WR ↑ | 250 | | 150 | | ns | |
| $t_{WD}$ | Data Hold After WR ↑ | 30 | | 0 | | ns | |

## A.C. TEST CONDITIONS

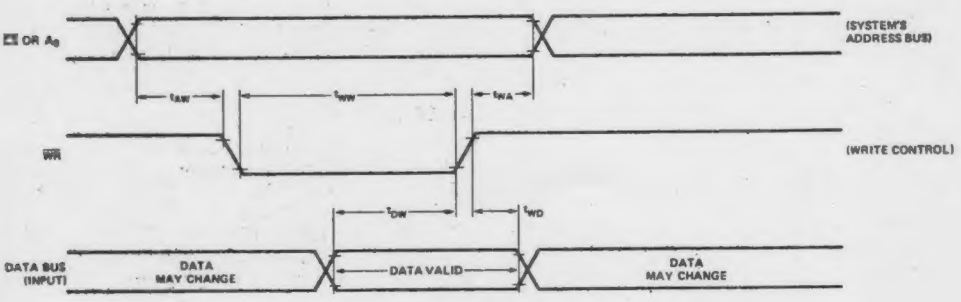
$D_7$-$D_0$ Outputs $R_L$ = 2.2k to $V_{SS}$
4.3k to $V_{CC}$
$C_L$ = 100 pF

## WAVEFORMS

**Read Operation — Data Bus Buffer Register**




**Write Operation — Data Bus Buffer Register**



## PIN DESCRIPTION

| Signal | Description |
|---|---|
| $D_0$-$D_7$ | Three-state, bi-directional, DATA BUS BUFFER lines used to interface the UPI-41 to an 8-bit master system data bus. |
| $P_{10}$-$P_{17}$ | 8-bit, PORT 1, quasi-bi-directional I/O lines. |
| $P_{20}$-$P_{27}$ | 8-bit, PORT 2, quasi-bi-directional I/O lines<br>The lower 4-bits ($P_{20}$-$P_{23}$) interface directly to the 8243 I/O expander device and contain address and data information during PORT 4-7 access. |
| $\overline{WR}$ | I/O write input which enables the master CPU to write data and command words to the UPI-41 DATA BUS BUFFER. |
| $\overline{RD}$ | I/O read input which enables the master CPU to read data and status words from the DATA BUS BUFFER or status register. |
| $\overline{CS}$ | Chip select input used to select one UPI-41 out of several connected to a common data bus. |
| $A_0$ | Address input used by the master processor to indicate whether byte transfer is data or command. |
| $T_0$, $T_1$ | Input pins which can be directly tested using conditional branch instructions.<br>$T_1$ also functions as the event timer input (under software control).<br>$T_0$ is used during PROM programming and verification in the 8741. |
| $X_1$, $X_2$ | Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency. |
| SYNC | Output signal which occurs once per UPI-41 instruction cycle. SYNC can be used as a strobe for external circuitry; it is also used to synchronize single step operation. |
| EA | External access input which allows emulation, testing and PROM/ROM verification. |
| PROG | Multifunction pin used as the program pulse input during PROM programming.<br>During I/O expander access the PROG pin acts as an address/data strobe to the 8243. |
| $\overline{RESET}$ | Input used to reset status flip-flops and to set the program counter to zero.<br>$\overline{RESET}$ is also used during PROM programming and verification. |
| $\overline{SS}$ | Single step input used in the 8741 in conjunction with the SYNC output to step the program through each instruction. |
| $V_{CC}$ | +5V power supply pin. |
| $V_{DD}$ | +5V during normal operation.Programming supply pin during PROM programming. Low power standby pin in ROM version. |
| $V_{SS}$ | Circuit ground potential. |

MPU PERIPHERALS

## UPI INSTRUCTION SET

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| **ACCUMULATOR** | | | |
| ADD A,Rr | Add register to A | 1 | 1 |
| ADD A,@Rr | Add data memory to A | 1 | 1 |
| ADD A,#data | Add immediate to A | 2 | 2 |
| ADDC A,Rr | Add immed. to A with carry | 1 | 1 |
| ADDC A,@Rr | Add immed. to A with carry | 1 | 1 |
| ADDC A,#data | Add immed. to A with carry | 2 | 2 |
| ANL A,Rr | AND register to A | 1 | 1 |
| ANL A,@Rr | AND data memory to A | 1 | 1 |
| ANL A,#data | AND immediate to A | 2 | 2 |
| ORL A,Rr | OR register to A | 1 | 1 |
| ORL A,@Rr | OR data memory to A | 1 | 1 |
| ORL A,#data | OR immediate to A | 2 | 2 |
| XRL A,Rr | Exclusive OR register to A | 1 | 1 |
| XRL A,@Rr | Exclusive OR data memory to A | 1 | 1 |
| XRL A,#data | Exclusive OR immediate to A | 2 | 2 |
| INC A | Increment A | 1 | 1 |
| DEC A | Decrement A | 1 | 1 |
| CLR A | Clear A | 1 | 1 |
| CPL A | Complement A | 1 | 1 |
| DA A | Decimal Adjust A | 1 | 1 |
| SWAP A | Swap digits of A | 1 | 1 |
| RL A | Rotate A left | 1 | 1 |
| RLC A | Rotate A left through carry | 1 | 1 |
| RR A | Rotate A right | 1 | 1 |
| RRC A | Rotate A right through carry | 1 | 1 |
| **INPUT/OUTPUT** | | | |
| IN A,Pp | Input port to A | 1 | 2 |
| OUTL Pp,A | Output A to port | 1 | 2 |
| ANL Pp,#data | AND immediate to port | 2 | 2 |
| ORL Pp,#data | OR immediate to port | 2 | 2 |
| IN A,DBB | Input DBB to A, clear IBF | 1 | 1 |
| OUT DBB,A | Output A to DBB, set OBF | 1 | 1 |
| MOVD A,Pp | Input Expander port to A | 1 | 2 |
| MOVD Pp,A | Output A to Expander port | 1 | 2 |
| ANLD Pp,A | AND A to Expander port | 1 | 2 |
| ORLD Pp,A | OR A to Expander port | 1 | 2 |
| **DATA MOVES** | | | |
| MOV A,Rr | Move register to A | 1 | 1 |
| MOV A,@Rr | Move data memory to A | 1 | 1 |
| MOV A,#data | Move immediate to A | 2 | 2 |
| MOV Rr,A | Move A to register | 1 | 1 |
| MOV @Rr,A | Move A to data memory | 1 | 1 |
| MOV Rr,#data | Move immediate to register | 2 | 2 |
| MOV @Rr,#data | Move immediate to data memory | 2 | 2 |
| MOV A,PSW | Move PSW to A | 1 | 1 |
| MOV PSW,A | Move A to PSW | 1 | 1 |
| XCH A,Rr | Exchange A and register | 1 | 1 |
| XCH A,@Rr | Exchange A and data memory | 1 | 1 |
| XCHD A,@Rr | Exchange digit of A and register | 1 | 1 |
| MOVP A,@A | Move to A from current page | 1 | 2 |
| MOVP3 A,@A | Move to A from page 3 | 1 | 2 |
| **TIMER/COUNTER** | | | |
| MOV A,T | Read Timer/Counter | 1 | 1 |
| MOV T,A | Load Timer/Counter | 1 | 1 |
| STRT T | Start Timer | 1 | 1 |
| STRT CNT | Start Counter | 1 | 1 |
| STOP TCNT | Stop Timer/Counter | 1 | 1 |
| EN TCNTI | Enable Timer/Counter Interrupt | 1 | 1 |
| DIS TCNTI | Disable Timer/Counter Interrupt | 1 | 1 |

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| **CONTROL** | | | |
| EN I | Enable IBF Interrupt | 1 | 1 |
| DIS I | Disable IBF Interrupt | 1 | 1 |
| SEL RB0 | Select register bank 0 | 1 | 1 |
| SEL RB1 | Select register bank 1 | 1 | 1 |
| NOP | No Operation | 1 | 1 |
| **REGISTERS** | | | |
| INC Rr | Increment register | 1 | 1 |
| INC @Rr | Increment data memory | 1 | 1 |
| DEC Rr | Decrement register | 1 | 1 |
| **SUBROUTINE** | | | |
| CALL addr | Jump to subroutine | 2 | 2 |
| RET | Return | 1 | 2 |
| RETR | Return and restore status | 1 | 2 |
| **FLAGS** | | | |
| CLR C | Clear Carry | 1 | 1 |
| CPL C | Complement Carry | 1 | 1 |
| CLR F0 | Clear Flag 0 | 1 | 1 |
| CPL F0 | Complement Flag 0 | 1 | 1 |
| CLR F1 | Clear F1 Flag | 1 | 1 |
| CPL F1 | Complement F1 Flag | 1 | 1 |
| **BRANCH** | | | |
| JMP addr | Jump unconditional | 2 | 2 |
| JMPP @A | Jump indirect | 1 | 2 |
| DJNZ R,addr | Decrement register and skip | 2 | 2 |
| JC addr | Jump on Carry = 1 | 2 | 2 |
| JNC addr | Jump on Carry = 0 | 2 | 2 |
| JZ addr | Jump on A Zero | 2 | 2 |
| JNZ addr | Jump on A not Zero | 2 | 2 |
| JT0 addr | Jump on T0 = 1 | 2 | 2 |
| JNT0 addr | Jump on T0 = 0 | 2 | 2 |
| JT1 addr | Jump on T1 = 1 | 2 | 2 |
| JNT1 addr | Jump on T1 = 0 | 2 | 2 |
| JF0 addr | Jump on F0 Flag = 1 | 2 | 2 |
| JF1 addr | Jump on F1 Flag = 1 | 2 | 2 |
| JTF addr | Jump on Timer Flag = 1, Clear Flag | 2 | 2 |
| JNIBF addr | Jump on IBF Flag = 0 | 2 | 2 |
| JOBF addr | Jump on OBF Flag = 1 | 2 | 2 |
| JBb addr | Jump on Accumulator Bit | 2 | 2 |

## APPLICATIONS

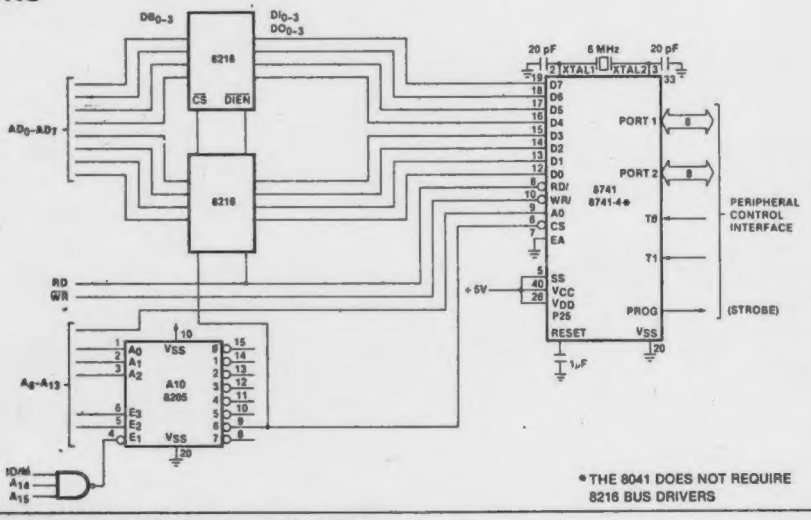



**Figure 1. Recommended 8741 Interface to an 8085 System**

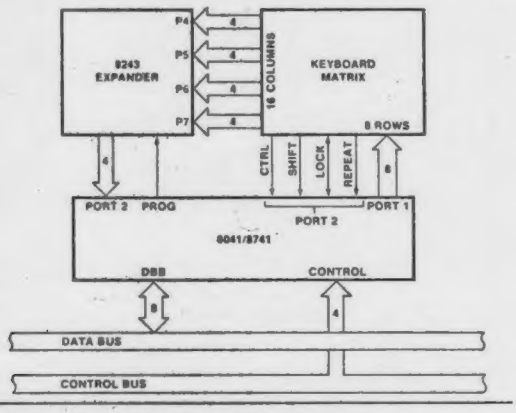



**Figure 2. 8041-8243 Keyboard Scanner**

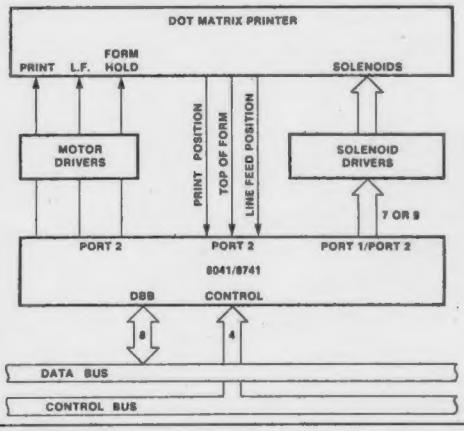



**Figure 3. 8041 Matrix Printer Interface**

## PROGRAMMING, VERIFYING, AND ERASING THE 8748 EPROM

### Programming/Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

| Pin | Function |
|---|---|
| XTAL 1 | Clock input (1 to 6 MHz) |
| RESET | Initialization and address latching |
| TEST 0 | Selection of program or verify mode |
| EA | Activation of program/verify modes |
| BUS | Address and data input data output during verify |
| P20-1 | Address input |
| $V_{DD}$ | Programming power supply |
| PROG | Program pulse input |

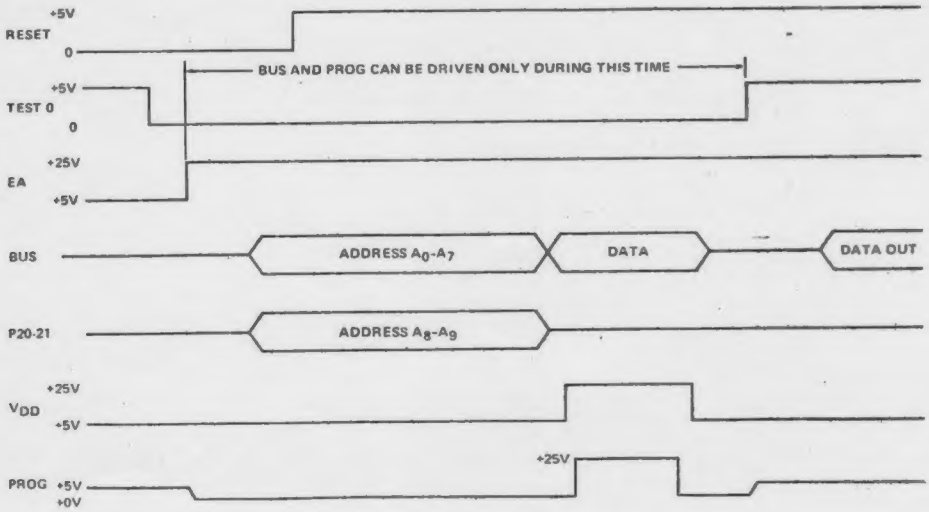
The program/verify sequence is:

1. $V_{DD}$ = 5V, clock applied or internal oscillator operating, RESET = 0V, TEST 0 = 5V, EA = 5V, BUS and PROG floating.
2. Insert 8748 in programming socket.
3. TEST 0 = 0V (select program mode).
4. EA = 25V (activate program mode).
5. Address applied to BUS and P20-1.
6. RESET = 5V (latch address).
7. Data applied to BUS.
8. $V_D$ = 25V (programming power).
9. PROG = 0V followed by one 50 ms pulse to 25V.
10. $V_{DD}$ = 5V.
11. TEST 0 = 5V (verify mode).
12. Read and verify data on BUS.
13. TEST 0 = 0V.
14. RESET = 0V and repeat from step 5.
15. Programmer should be at conditions of step 1 when 8748 is removed from socket.

### Programming Options

The 8748 EPROM can be programmed by either of two Intel products:

1. PROMPT-48 Microcomputer Design Aid.
2. Universal PROM Programmer (UPP-101 or UPP-102) Peripheral of the Intellec® Development System with a UPP-848 Personality Card.




WARNING: An attempt to program a missocketed 8748 will result in severe damage to the part. An indication of a properly socketed part is the appearance of the ALE clock output. The lack of this clock may be used to disable the programmer.

**Figure 5. Programming/Verification Sequence**

### 8748 Erasure Characteristics

The erasure characteristics of the 8748 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (A). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 8748 in approximately 3 years while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 8748 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8748 window to prevent unintentional erasure.

The recommended erasure procedure for the 8748 is exposure to shortwave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 W-sec/cm$^2$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 $\mu$W/cm$^2$ power rating. The 8748 should be placed within one inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

## A.C. TIMING SPECIFICATION FOR PROGRAMMING

$T_A$ = 25°C ±5°C, $V_{CC}$ = 5V ±5%, $V_{DD}$ = 25V ±1V

| Symbol | Parameter | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| $t_{AW}$ | Address Setup Time to $\overline{\text{RESET}}$ ↑ | 4tCY | | | |
| $t_{WA}$ | Address Hold Time After $\overline{\text{RESET}}$ ↑ | 4tCY | | | |
| $t_{DW}$ | Data in Setup Time to PROG ↑ | 4tCY | | | |
| $t_{WD}$ | Data in Hold Time After PROG ↓ | 4tCY | | | |
| $t_{PH}$ | $\overline{\text{RESET}}$ Hold Time to Verify | 4tCY | | | |
| $t_{VDDW}$ | $V_{DD}$ | 4tCY | | | |
| $t_{VDDH}$ | $V_{DD}$ Hold Time After PROG ↓ | 0 | | | |
| $t_{PW}$ | Program Pulse Width | 50 | 60 | MS | |
| $t_{TW}$ | Test 0 Setup Time for Program Mode | 4tCY | | | |
| $t_{WT}$ | Test 0 Hold Time After Program Mode | 4tCY | | | |
| $t_{DO}$ | Test 0 to Data Out Delay | | 4tCY | | |
| $t_{WW}$ | $\overline{\text{RESET}}$ Pulse Width to Latch Address | 4tCY | | | |
| $t_r$, $t_f$ | $V_{DD}$ and PROG Rise and Fall Times | 0.5 | 2.0 | $\mu$s | |
| $t_{CY}$ | CPU Operation Cycle Time | 5.0 | | $\mu$s | |
| $t_{RE}$ | $\overline{\text{RESET}}$ Setup Time Before EA ↑ | 4tCY | | | |

Note: If TEST 0 is high, $t_{DO}$ can be triggered by $\overline{\text{RESET}}$ ↑.

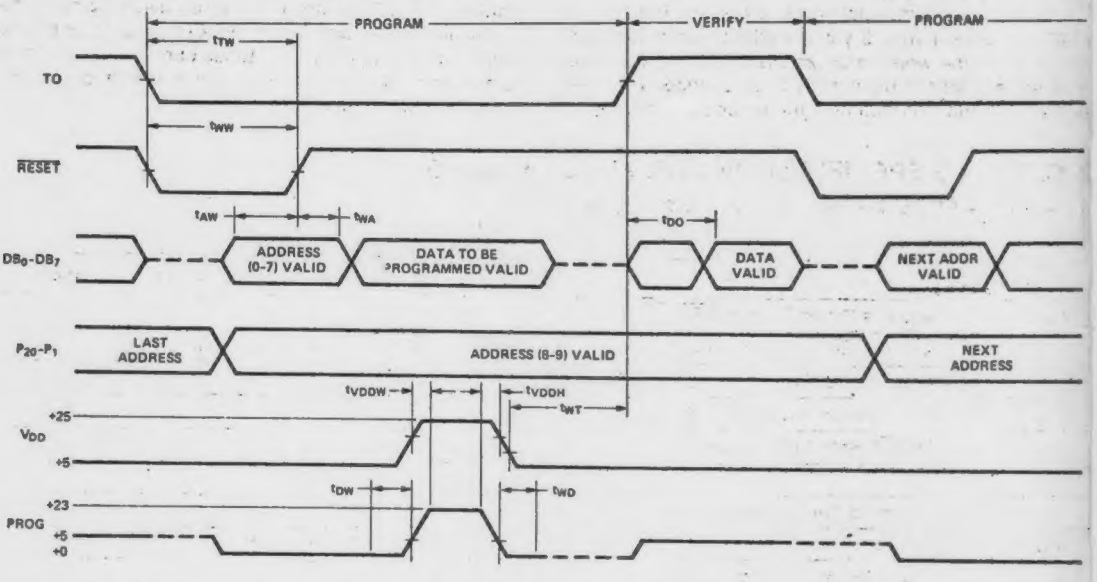
## D.C. SPECIFICATION FOR PROGRAMMING

$T_A$ = 25°C ±5°C, $V_{CC}$ = 5V ±5%, $V_{DD}$ = 25V ±1V

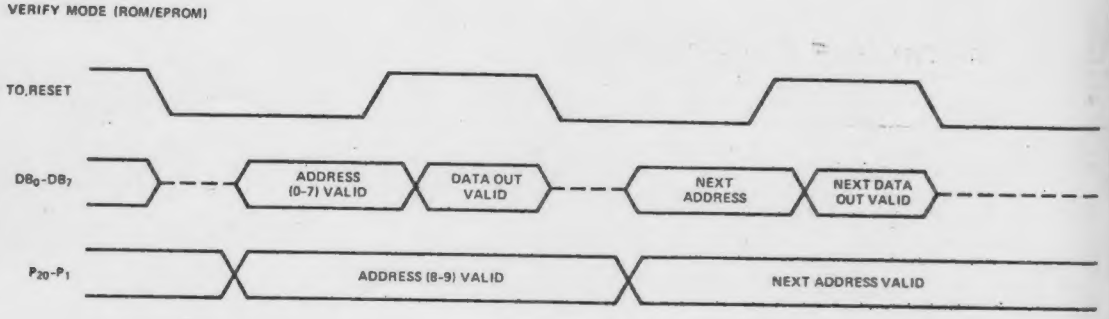
| Symbol | Parameter | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{DOH}$ | $V_{DD}$ Program Voltage High Level | 24.0 | 26.0 | V | |
| $V_{DDL}$ | $V_{DD}$ Voltage Low Level | 4.75 | 5.25 | V | |
| $V_{PH}$ | PROG Program Voltage High Level | 21.5 | 24.5 | V | |
| $V_{PL}$ | PROG Voltage Low Level | | 0.2 | V | |
| $V_{EAH}$ | EA Program or Verify Voltage High Level | 21.5 | 24.5 | V | |
| $V_{EAL}$ | EA Voltage Low Level | | 5.25 | V | |
| $I_{DD}$ | $V_{DD}$ High Voltage Supply Current | | 30.0 | mA | |
| $I_{PROG}$ | PROG High Voltage Supply Current | | 16.0 | mA | |
| $I_{EA}$ | EA High Voltage Supply Current | | 1.0 | mA | |

## WAVEFORMS

### Combination Program/Verify Mode (EPROMs Only)




### Verify Mode (ROM/EPROM)




MPU PERIPHERALS